DESCRIPTION

The PT2466 is a monolith integrated motor driver designed for gauge valves control, toy or power electronic locks. The overall performance is optimized for low supply voltage, battery-powered applications.

The superior low switches resistance (RDSon) minimized the power dissipates, therefore a small DFN and SOP-8 package is available for high current output, to prevent un-determinates miss operation, overall protections function was integrated such like over-current, under-voltage lockout and over temperature protection.

FEATURE

- Single H-bridge driver could drive DC brushed Motor or solenoid loads.
- 1.8 Amps maximum DC output current
- Low power switches resistance: 0.28Ω,high and low side both
- Dual supply power supply:
  - For control logic (VCC) : 1.8V ~ 6V
  - For motor drives (VM) : 0 to 12V
- Low power shutdown mode:
  - Less than 10nA on all supply rail.
- Small Footprint Package
  - 8-Pin DFN with Thermal PAD (2.0 X 2.0 mm)
  - 8-Pin SOP
- Fully protection function includes VCC under voltage lockout (UVLO), over current protection and thermal shutdown.

APPLICATION

- Gauge valves
- Motor powered lenses
- Electronic locks
- Toys
- Robotics

BLOCK DIAGRAM

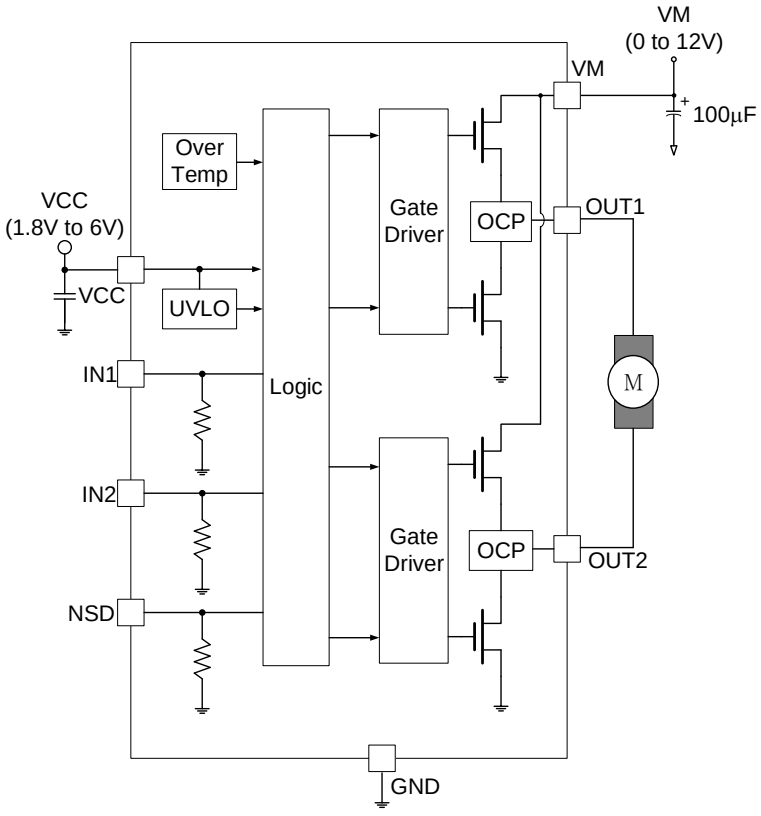


Figure 1. Function Block Diagram

APPLICATION CIRCUIT

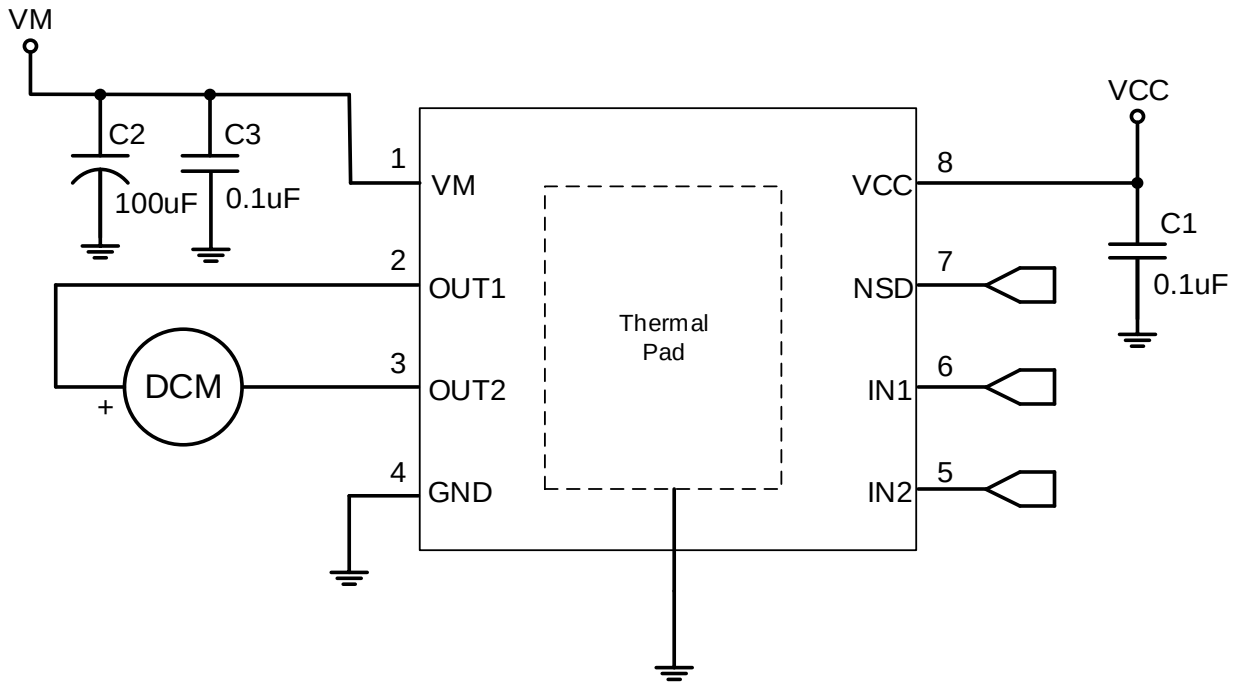


Figure 2. Schematic of Application

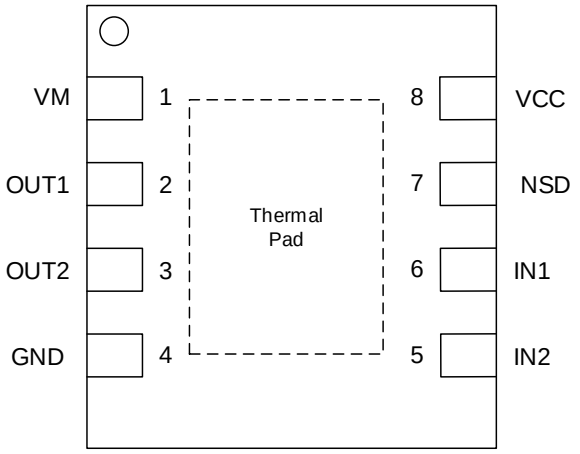
(Please refer to page 5 for bypass capacitor and PCB layout recommendation.)

ORDER INFORMATION

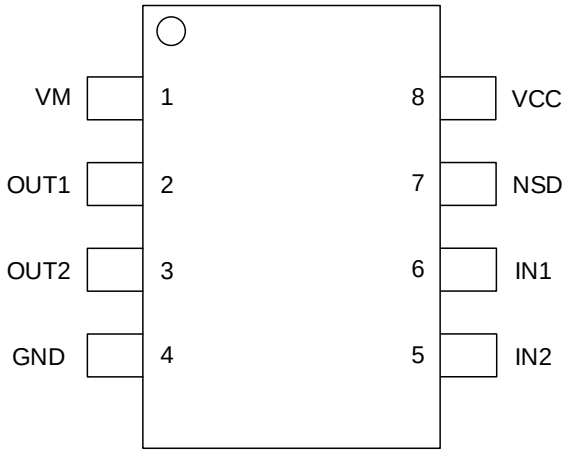
Valid Part Number	Package Type	Top Code
PT2466-S	8-Pin, SOP, 150 MIL	PT2466-S
PT2466	8-Pins, DFN	2466

PIN DESCRIPTION

DFN-8



SOP-8



Pin Name	I/O	Description	Pin No.
VM	POWER	Power supply for motor drives	1
OUT1	OUTPUT	H-bridge output 1	2
OUT2	OUTPUT	H-bridge output 2	3
GND	POWER	Ground	4
IN2	INPUT	Control logic input 2	5
IN1	INPUT	Control logic input 1	6
NSD	INPUT	Shutdown control input	7
VCC	POWER	Power supply for control logic	8

FUNCTION DESCRIPTION

H-BRIDGE OUTPUT DEFINITION

The output current of H-bridge driver is determinate by control logic interface; it also called a dual input interface (IN-IN). Please refer to Table 1 for corresponds between input and output.

NSD	IN1	IN2	OUT1	OUT2	DC Motor Operates
0	X	X	HiZ	HiZ	Coast
1	0	0	HiZ	HiZ	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

Table 1. H-Bridge Output Definition

FUNCTIONAL AND PROTECTION OPERATES

The PT2466 equipped fully protection function; please refer to the Table 2 for detail descriptions.

Function Operation	Criteria	H-Bridge Outputs
VCC under-voltage	VCC < 1.7V	All outputs disable
	VCC >1.8V	Normal operates
Output over-current or short circuits, Includes shorted to VM, GND and cross load.	IOUT < 1.8A	Normal operates
	IOUT > 1.9A	All outputs disable for a short period (tRETRY) and release, this reaction will repeating until short circuits is removed.
Die temperature exceeds Thermal Shutdown limits	T_J < 160℃	Normal operates
	T_J > 160℃	All outputs disable and it will returns to normal operation until die temperature is lower than threshold.
Power saving mode	NSD = H	Normal operates
	NSD = L	All outputs disable and supply currents reduced to under 10nA.

Table 2. Functions Behavior

POWER SUPPLY CAPACITOR RECOMMENDATIONS

Consider a real world application scenario; the motor driver is designed to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor.

In another case, the parasitic reactance (inductance + resistance) of power wire between the power supply and motor driver board with parasitic capacitance of PCB consists a LC resonates tank, during power supply sourcing current to the motor driver board, the VM voltage may drops quickly and parasitic LC will be trigged and shows oscillation spike if the local bypass capacitor is not sufficient.

To prevent unstable bounce or spike appears on VM bus, a high capacitance bounce absorber capacitor (>100μF) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC 0.1μF bypass capacitor should be placed near the motor driver IC power pin, VM and VCC both, to reduce the spike causes by power line LC resonates.

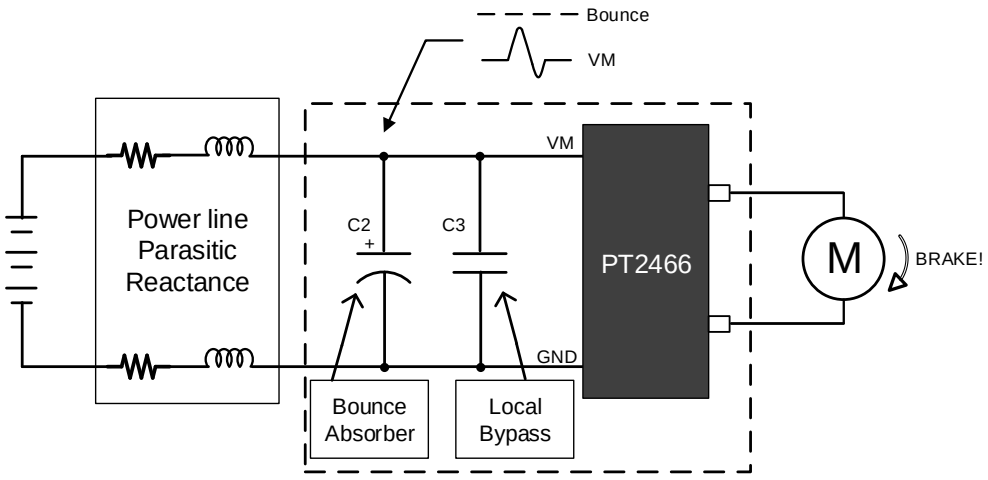


Figure 3. Motor Driver System with External Power Supply

PCB LAYOUT RECOMMENATION

The local bypass capacitor C1 and C3 should be placed near the IC power pins, and bounce absorber capacitor C2 should be placed on VM bus line. The GND plane should be placed on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance(θ_{JA}). The thermal pad under DFN package should be soldered to the PCB component side and connects to the bottom side through the via holes, this arrangement can further enhance the heat dissipation.

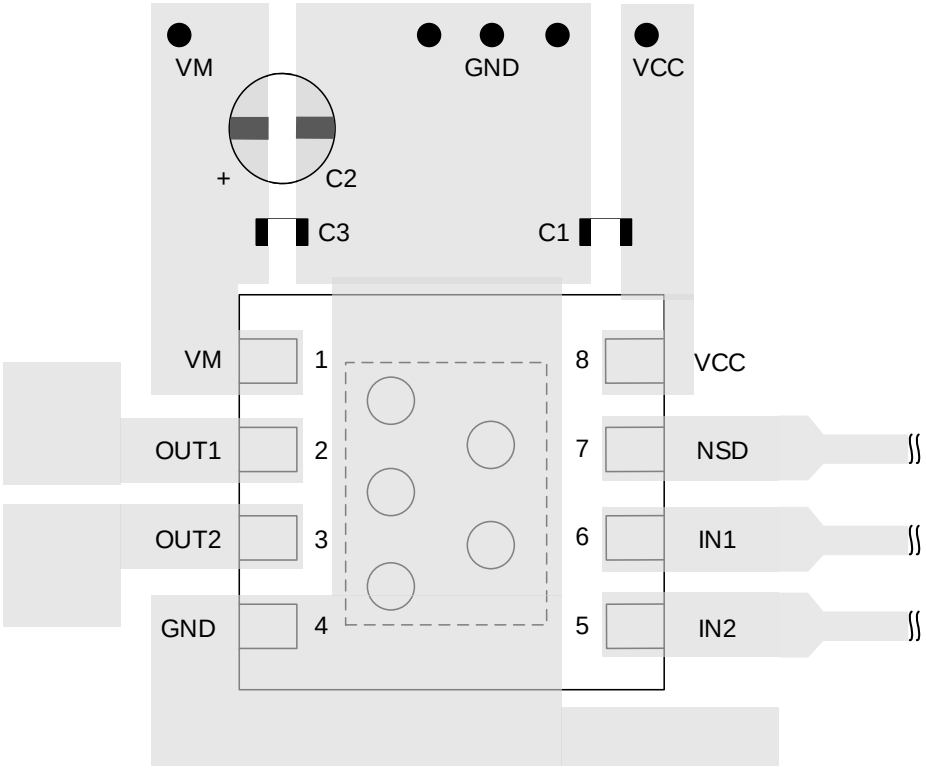


Figure 4. Simplified Layout Example

ABSOLUTE MAXIMUM RATINGS

Parameters			Min	Max	Unit
Motor power supply voltage , VM			-0.3	13	V
Logic power supply voltage , VCC			-0.3	6.5	V
Operating Temperature, Top			-40	150	°C
Storage Temperature, Tstg			-40	150	°C
Operation Humidity			20	85	%
Storage Humidity			20	90	%
ESD	All Pins	HBM	±4		KV
		MM	±0.4		KV
		CDM*	±1.5		KV

*CDM test is based on ANSI/ESDA/JECEC JS-002-2014

RECOMMENDED OPERATING CONDITIONS

Parameters		Min	Max	Unit
VM	Motor power supply voltage	0	12	V
VCC	Logic power supply voltage	1.8	6	V
I_{OUT}	Motor peak current	0	1.8	A
f_{PWM}	Externally applied PWM frequency	0	250	KHz
V_{LOGIC}	Logic level input voltage	0	6	V
T_A	Operating ambient temperature	-40	85	°C

PACKAGE THERMAL CHARACTERISTICS

PACKAGE: DFN

Parameter	Symbol	Value	Unit
From chip conjunction dissipation to external environment	θJA	75.6	℃/W

PACKAGE: SOP, 150MIL

Parameter	Symbol	Value	Unit
From chip conjunction dissipation to external environment	θJA	113.9	℃/W

ELECTRICAL CHARACTERISTICS

T_A=25℃ , over recommended operating conditions unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supplies(VM, VCC)						
VM Current						
I_{VM1}	VM coast current	VM=5V ; VCC=3V ; No PWM Coast Mode		65	90	μA
I_{VM2}	VM F/R current	VM=5V ; VCC=3V ; No PWM Forward/Reverse Mode		300	500	μA
I_{VM3}	VM brake current	VM=5V ; VCC=3V ; No PWM Brake Mode		65	90	μA
I_{VM4}	VM PWM current	VM=5V ; VCC=3V PWM=50KHz		240	400	μA
I_{VMQ}	VM sleep current	VM=5V ; VCC=3V NSD=L		5		nA
VCC Current						
I_{VCC1}	VCC coast current	VM=5V ; VCC=3V ; No PWM Coast Mode		380	500	μA
I_{VCC2}	VCC F/R current	VM=5V ; VCC=3V ; No PWM Forward/Reverse Mode		450	650	μA
I_{VCC3}	VCC brake current	VM=5V ; VCC=3V ; No PWM Brake Mode		480	650	μA
I_{VCC4}	VCC PWM current	VM=5V ; VCC=3V PWM=50KHz		450	650	μA
I_{VCCQ}	VCC shutdown current	VM=5V ; VCC=3V, NSD=L		2		nA
Control Logic Inputs (IN1, IN2, NSD)						
V_{IL}	Input logic low voltage				0.3*VCC	V
V_{IH}	Input logic high voltage		0.5*VCC			V
I_{IL}	Input logic low current	V_{IN}=0V			5	μA
I_{IH}	Input logic high current	V_{IN}=3.3V			50	μA
R_{PD}	Pulldown resistance	IN1, IN2, NSD		100		KΩ
***H-Bridge Driver Outputs* (OUT1, OUT2)**						
$RDS_{(ON)}$	HS + LS switch ON resistance	VM=5V ; VCC=3V ; Io=800mA ; Tj=25℃		280		mΩ
I_{OFF}	Off-state leakage current	Output=OPEN		5		nA
Protections						
V_{UVLO}	VCC under-voltage lockout	VCC falling			1.7	V
		VCC rising	1.8			V
I_{OCP}	Over-current protection trip level		1.9		3.5	A
t_{RETRY}	Over-current retry time			1		mS
T_{OTP}	Thermal shutdown temperature	Die temperature		160		℃
I/O Propagation Delay and Timing Requirement						
Ten	Output enable time	TA=25℃, VM=5V, VCC=3V, RL=47Ω			0.8	μS
Tdis	Output disable time				0.8	μS
Tdh	Delay time, INx high to OUTx high				0.7	μS
Tdl	Delay time, INx low to OUTx low				0.7	μS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Tr	Output rise time				0.5	µS
Tf	Output fall time				0.5	µS
Tsdn	Wake time , NSD rising edge to output active				5	µS

TIMING CHART

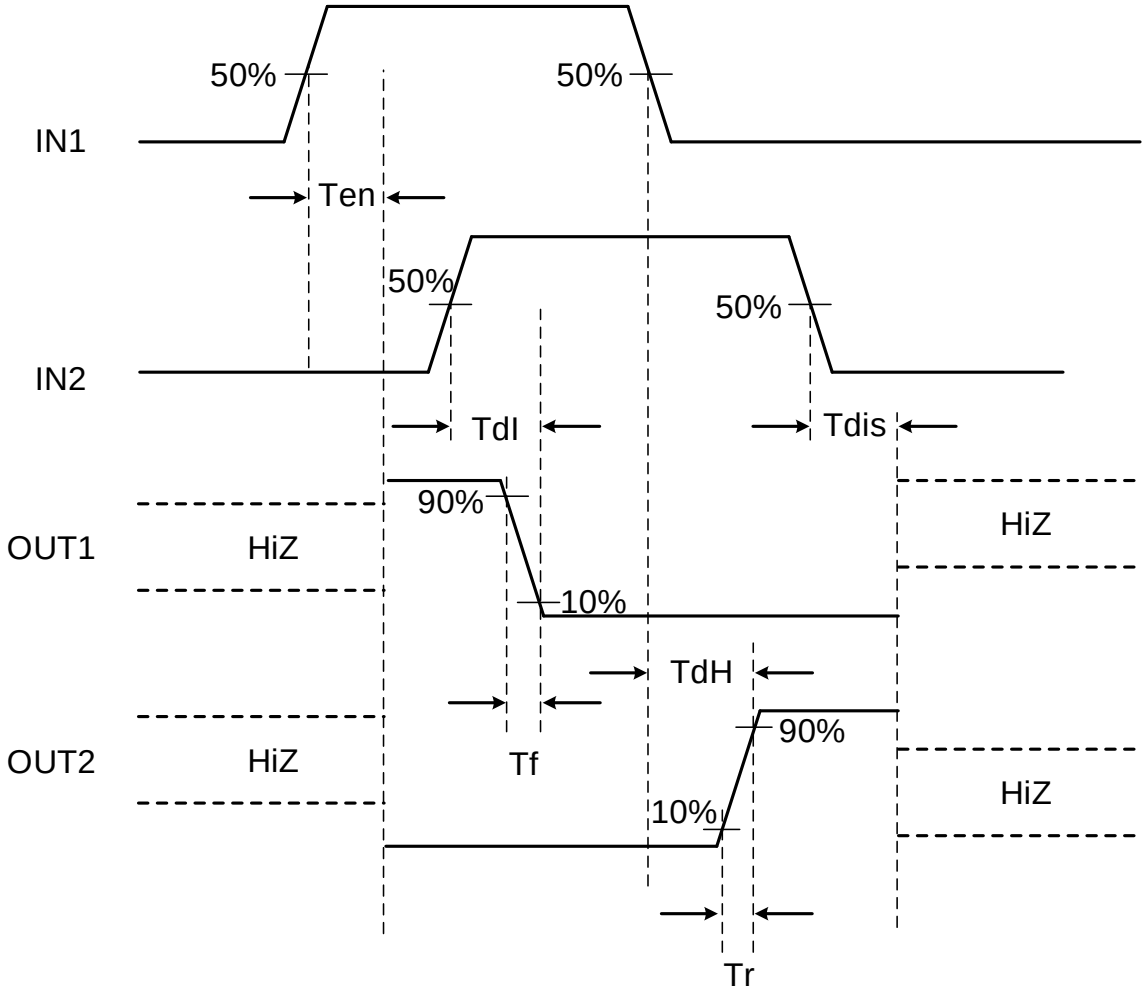


Figure 5. Input and Output Timing

TYPICAL OPERATING CHARACTERISTICS

(VM=5V, VCC=3V unless otherwise noted)

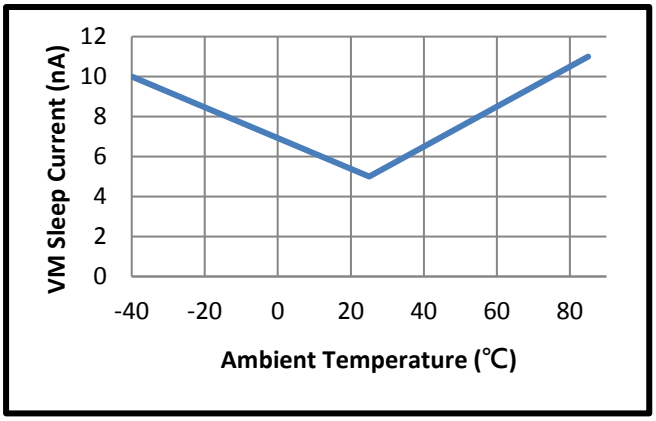


Figure 6. I_{VMQ} vs T_A

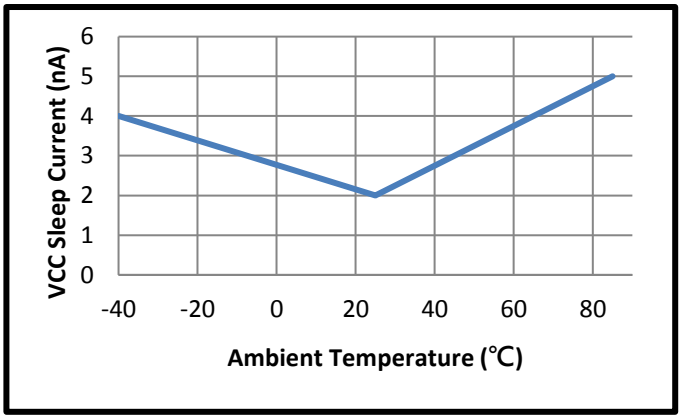


Figure 7. I_{VCCQ} vs T_A

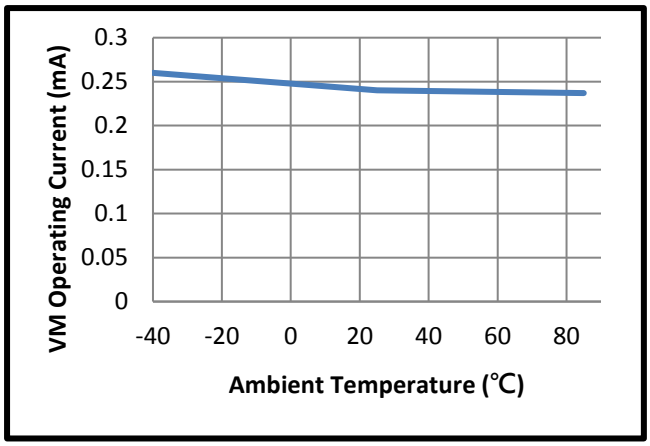


Figure 8. I_{VM} vs T_A (50KHz PWM)

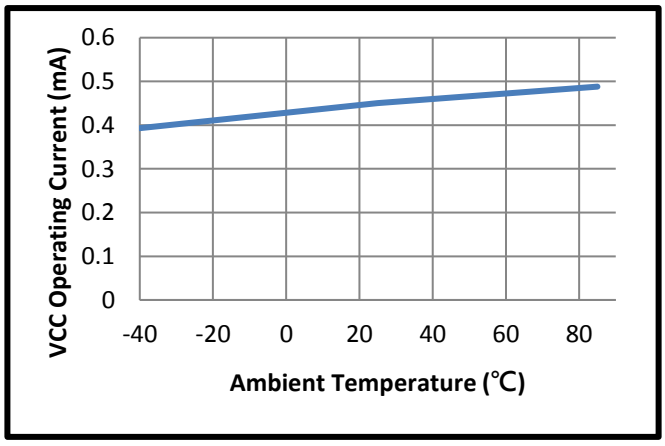


Figure 9. I_{VCC} vs T_A (50KHz PWM)

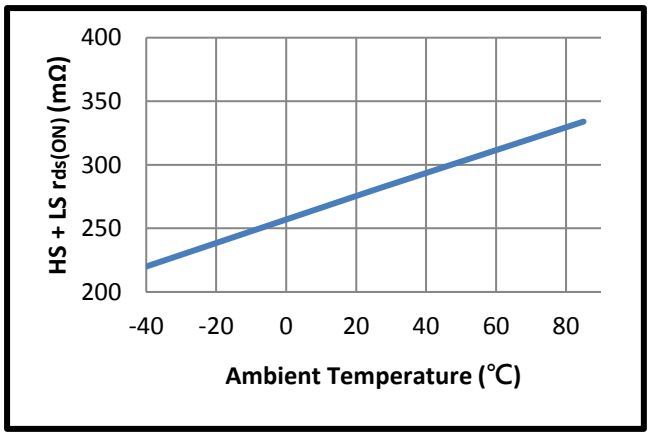


Figure 10. HS + LS r_{DS}-on vs T_A

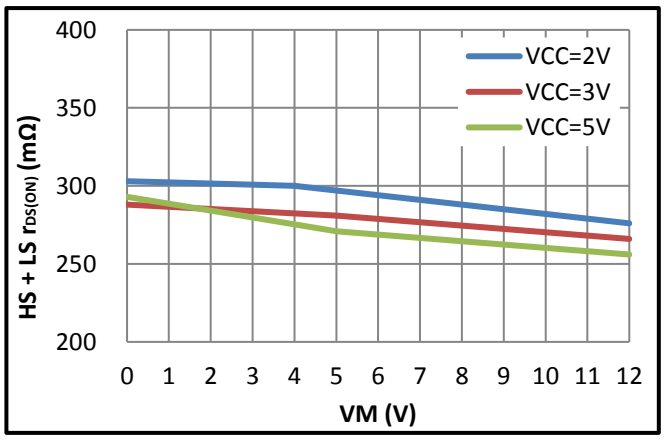


Figure 11. HS + LS r_{DS}-on vs VM

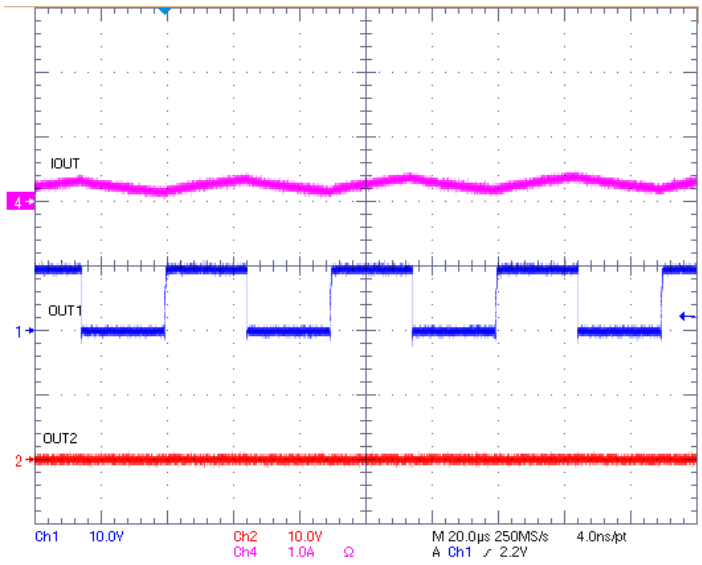


Figure 12. 50% Duty Cycle , Forward Direction

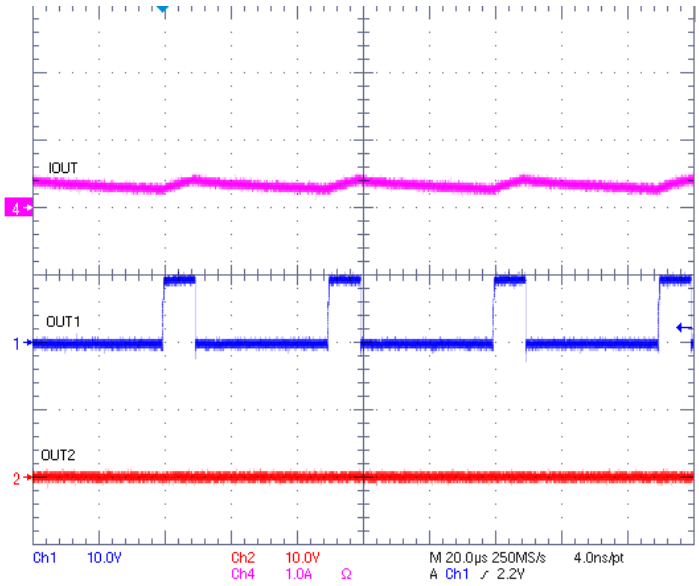


Figure 13. 20% Duty Cycle , Forward Direction

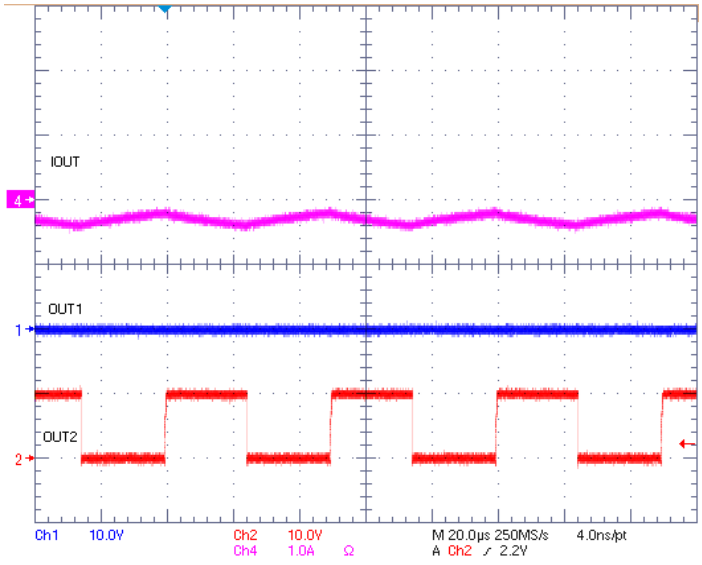


Figure 14. 50% Duty Cycle , Reverse Direction

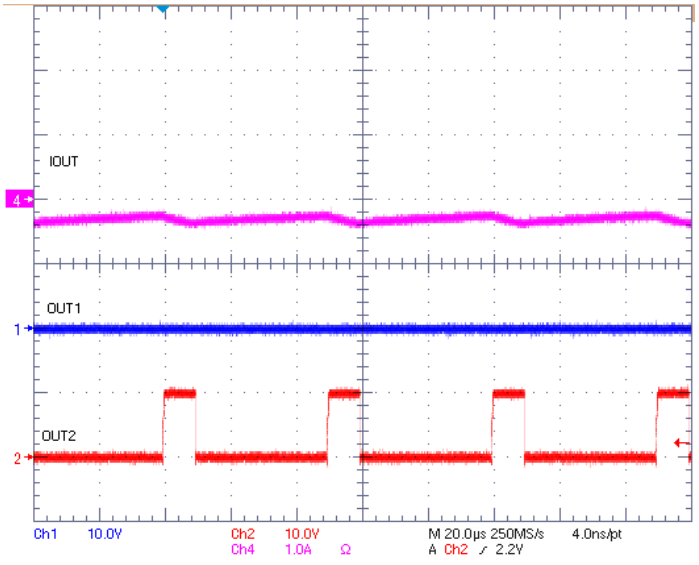
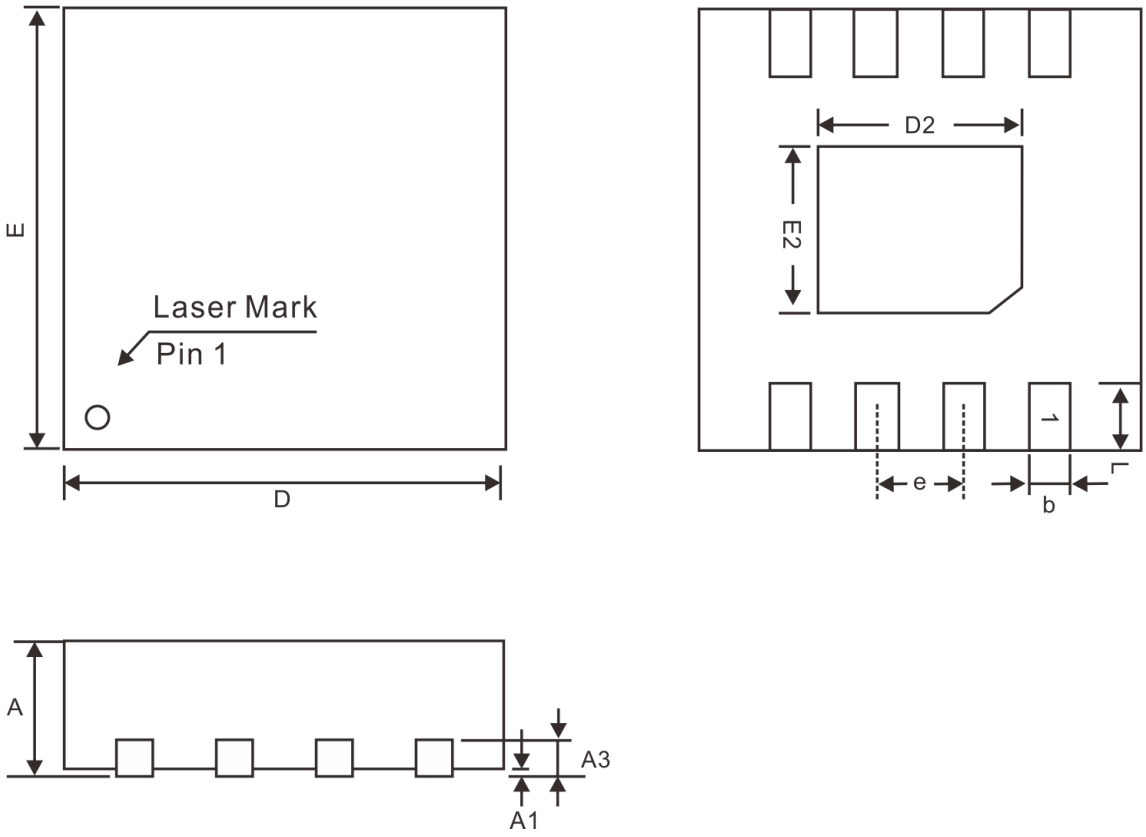


Figure 15. 20% Duty Cycle , Reverse Direction

PACKAGE INFORMATION

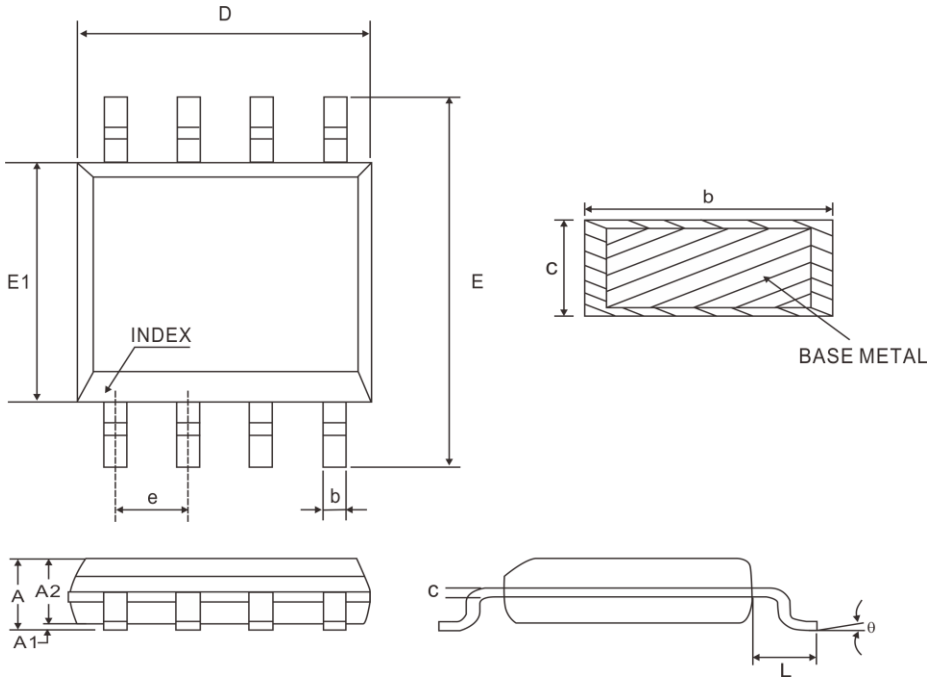
8-PIN, DFN



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		2.00 BSC	
E		2.00 BSC	
e		0.50 BSC	
D2	1.50	1.60	1.65
E2	0.80	0.90	0.95
L	0.25	0.30	0.35

Note: Refer to JEDEC MO-229

8 PINS, SOP, 150MIL



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27BSC		
L	0.40	-	1.27
θ	0°	-	8°

Notes: Refer to JEDEC MS-012 AA

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